SUBTHRESHOLD LEAKAGE REDUCTION TECHNIQUES FOR LOW POWER CMOS CELL LIBRARY

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A SYNOPSIS/ RESEARCH PROPOSAL

SUBMITTED TO THE

SHRI JAGDISH PRASAD JHABARMAL TIBREWALA UNIVERSITY,

FOR THE DEGREE
OF

DOCTOR OF PHILOSOPHY

IN

ELECTRONICS

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REGISTRATION NO.:- 10110200

UNDER THE GUIDANCE OF

Dr.ARTI NOOR

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

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YEAR-2012

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INTRODUCTION

Historically, VLSI designers have focused on increasing the speed and reducing the area of digital systems. However, the evolution of portable systems and advanced Deep Sub-Micron fabrication technologies has brought power dissipation as another critical design factor[1]. Low power design reduces cooling cost and increases reliability especially for high density systems. Moreover, it reduces the weight and size of portable devices. The power dissipation in CMOS circuits consists of static and dynamic components. Since dynamic power is proportional to V^2_{dd} and static power is proportional to V_{dd}, lowering the supply voltage and device dimensions, the transistor threshold voltage also has to be scaled down to achieve the required performance. Due to the exponential nature of leakage current in subthreshold region of the transistor, the leakage current can no longer be ignored. In this paper we have been proposed the new CMOS library for the complex digital design using scaling the supply voltage and device dimensions and also suggest the methods to control the leakage current to obtain the minimum power dissipation at optimum value of supply voltage and transistor threshold[4].

Recently advances in VLSI Technology have made it possible to put a complete System on Chip (SOC) which facilitates the developments of PDAs, Laptop, cellular phones etc. The evolutions of these applications profiles power dissipation as a critical parameter in digital VLSI design[2]. Power dissipation is defined as the rate of energy delivered from the source to the system/devices. In battery operated systems, the amount of energy stored within the battery is limited. Therefore, the power dissipation is important for portable systems, as it defines the average lifetime of the battery. Power dissipation is also crucial for Deep Sub Micron technologies[22]. Advances in CMOS fabrication technology double the number of transistors per chip every two years and double

the operating frequency every three years. Consequently, the power dissipation per unit area grows, increasing the chip temperature. Hence large cooling devices and special packaging are required to dissipate the extra heat[6].

Power dissipation in CMOS digital circuits is categorized into two types: **peak power and average power**. Peak power affects both circuit lifetime and performance. Average power dissipation is significant for calculating the battery weight and lifetime. Average power is categorized into: **dynamic power and static power dissipation**. Dynamic power is the component proportional to the operating frequency of the circuit or the frequency of the node switching so it is more important during the normal operations whereas the static power is independent of the frequency so it is more important for battery operated devices[22].

In Dynamic power dissipation, the average switching power consumption of gate is given by:

$$P_{switch} = \alpha_i C_i V_{dd}^2 f \quad - \quad (1)$$

In CMOS circuit the short circuit power is a result of the transient current that flows between Vdd and ground when both the NMOS and PMOS devices are turned on during logic transitions if **Isc** is the mean short circuit current drawn by a CMOS gate over a finite period of time T, then the average short circuit power **Psc** is given as:

$$P_{sc} = I_{SC} \times V_{dd} \quad - \quad (2)$$

In case of **static power** the power is consumed during the steady state condition i.e when there are no input/output transitions. Static power has two sources: DC power and Leakage power.

The first component is an inherent property of some CMOS circuit styles, while the second is an outcome of the fact that a MOS transistor is not a perfect switch and so leaks some current[19].

In past day's technology the magnitude of leakage current was low and usually neglected. In current trends, the supply voltage is being scaled down to reduce dynamic power and MOS field-effect transistors (MOSFETs) with low threshold voltages (Vth) have to be used. This could be inferred as

lower the threshold voltage, lower the degree to which MOSFETs in logic gates are turned off and higher is the standby leakage current [10]. Scaling down of Vth, leads to an exponential increase in subthreshold leakage current. Subthreshold leakage current is the drain-to-source leakage current when the transistor is OFF. This happens when the applied gate to source voltage Vgs is less than threshold voltage Vth of transistor (weak inversion mode).

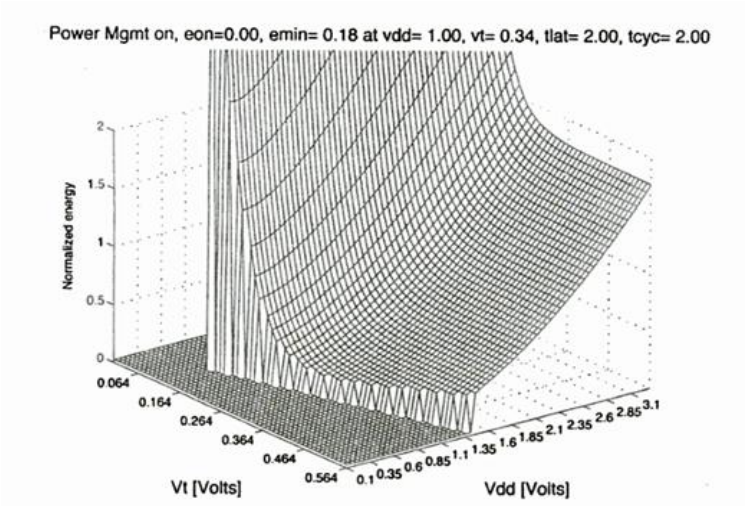

Fig1.Power dissipation as function of supply voltage (Vdd) and Threshold voltage (Vth)

The Sub-threshold current flows due to diffusion current of minority carriers in the channel of MOSFET. The following equation-1 relates subthreshold current ISUB with other device parameters [14].

$$I_{SUB} = I_o e^{(Vgs- Vth-\eta Vds-\gamma Vsb/\eta Ve)} (1-e^{-Vth/Ve}) \qquad ----(3)$$

$$Io = \mu C_{ox}(W/L).V^2_{\varphi} e^{1.8} \text{ ----------(4)}$$

where, Cox is the gate oxide capacitance per unit area, μ denotes carrier mobility, W and L denote the width and length of the transistor,VΘ=kT/q is the thermal voltage, γ is body effect coefficient, η denotes the drain-induced barrier lowering coefficient, n is the slope shape factor sub-threshold swing coefficient.

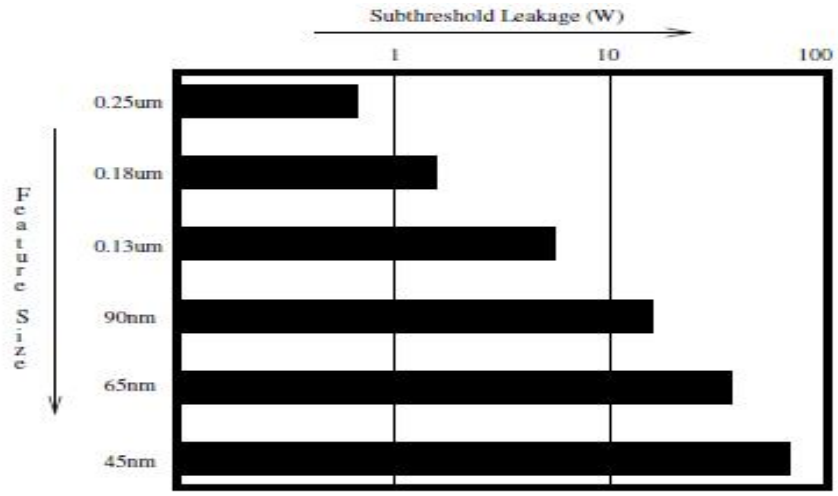

Fig2. Subthreshold leakage power trends

In order to facilitate voltage scaling without affecting the performance, threshold voltage has to be reduced. This also leads to better noise margins and helps to avoid the hot carrier effects in short channel devices. Scaling down of threshold voltage results in exponential increase of the subthreshold leakage current[13]. So, before going to in nanometer regime we need some techniques applied for CMOS logic to minimize the leakage power.

Historical Perspective of Low power

But by what metric should “performance” be measured, and what factors will influence “cost”? Historically, system performance has been synonymous with circuit speed or processing power. For example, in the microprocessor world, performance is often measured in Millions of Instructions Per Second (MIPS) or Millions of Floating point Operations Per Second (MFLOPS).In other words, the highest “performance” system is the one that can perform the most computations in a given amount of time. Likewise, in the analog domain, bandwidth (a frequency-domain measure of circuit speed) is a common performance metric[15]. The question of cost really depends on the implementation strategy being considered. For integrated circuits there is a fairly direct correspondence between silicon area and cost. Increasing the implementation area tends to

result in higher packaging costs as well as reduced fabrication yield with both effects translating immediately to increased product cost. Moreover, improvements in system performance generally come at the expense of silicon real estate. So, historically, the task of the VLSI designer has been to explore the Area-Time (AT) implementation space, attempting to strike a reasonable balance between these often conflicting objectives[27]. But area and time are not the only metrics by which we can measure implementation quality. Power consumption is yet another criterion. Until recently, power considerations were often of only secondary concern - taking the back seat to both area and speed. Of course, there are exceptions to this rule; for example, designers of portable devices such as wrist watches have always placed considerable emphasis on minimizing power in order to maximize battery life. For the most part, however, designers of mainstream electronic systems have considered power consumption only as an afterthought - designing for maximum performance regardless of the effects on power[29].

The tremendous growth in the semiconductor industry over the last two decades has largely been a result of the scaling of CMOS devices which, over the years, has yielded lower costs with more die per wafer, smaller feature sizes and increased performance. However, device scaling has reached a point of threshold today, wherein its benefits are realized only if a device’s power consumption can be reduced by a few orders of magnitude.

Power minimization is of paramount importance for designers today, especially in the portable electronic-device market, where devices have become increasingly feature rich and power hungry.Low supply voltages play a significant role in determining the power consumption in portable electronic-device circuits.

Power Reduction techniques for CMOS

1 Low power circuit techniques

Since switching power is the dominant power sink in CMOS circuits, several techniques have been proposed to reduce this power dissipation[19]. The techniques are :-

1. Supply Voltage Scaling

2. Reducing Effective Capacitance

3. Reduce output voltage swing

4. Switching Activity Reduction

2 Low power Gate level Design

Gate level design is the process of transforming the RTL code into gate level net list. The following methods are used to reduce power dissipation at this level[22]:

1. Low Power Synthesis

2. Gate sizing

3. Rescheduling

4. Clock Gating

5. Effects on circuit style

3 Low Power Behavioral Design

Behavioral design is the mapping of system block level into RTL coding using an HDL language. In this method power dissipation may be reduced by the following method:

1. Parallelism and Pipelining

2. Glitch Reduction

3. Multiple supply voltages

4. Non overlapping clocks

5. Reducing the memory Access

4 Low Power System Design

System level is the highest level of abstraction in to the digital system. Modification on the system level has the most impact on the quality of implementation [30]. These techniques are critical because of their effect on design analysis, synthesis automated layout and testing. The methods are:-

1. Sleep and Power down modes
2. Adaptive filtering
3. Dynamically varying the threshold voltage
4. Performance Management

Subthreshold leakage Reduction techniques

Many modifications may be applied to the process technology in order to reduce power dissipation. Power consumption (Static) of CMOS circuits in static condition is becoming a major challenge in UDSM technologies which was ignored in earlier CMOS technologies [33]. The following techniques are used to reduce the leakage:-

1. Threshold leakage reduction
2. Technology Scaling
3. SOI
4. MTCMOS (Multithreshold CMOS) devices
4. VTCMOS (Variable threshold CMOS Device)
5. LBFF (Low bias feed back flip flop)
6. Switch Source Impedance

Brief review of the available technologies

a) Switch Source Impedance

One obvious method for reducing leakage current is to decrease *VGS* in standby mode by raising the source voltage through switched-source-impedance CMOS [3]. In this approach, a passive

resistor is switched in between a gate's source nodes and ground during standby mode. During active mode, the resistor is shorted out so that there is no additional delay penalty.

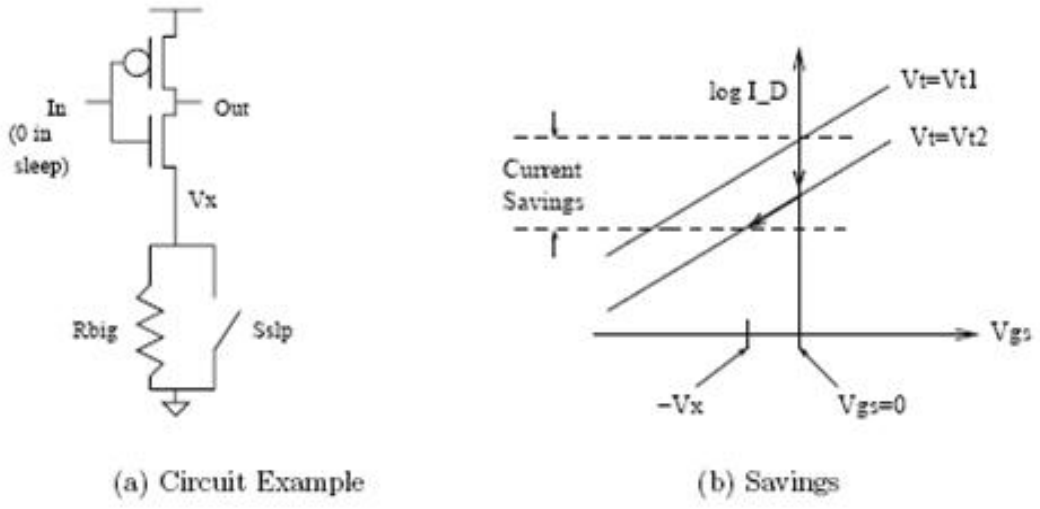

Figure 3 Circuit of switched source impedance

b)Multi Threshold Complementary Metal Oxide Semiconductor

Multi-Threshold CMOS (MTCMOS) refers to a circuit technique that uses a highVT footer and/or header FET to sever a circuit from the power rails . Turning off the high VT devices in standby mode places at least one high VT FET on each path from power to ground, thereby reducing the leakage current significantly. Sizing the sleep devices is no easy task. Small sleep devices further reduce the leakage current in standby mode but slow down transitions in active mode. The loss of performance occurs because smaller sleep devices sink less current through to ground.

Despite some of the design difficulties, MTCMOS techniques appear to be viable for reducing leakage currents in new technologies [16].

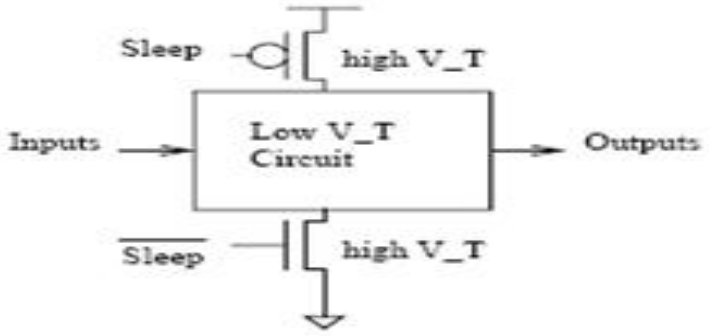

Figure 4 MTCMOS Circuit

c) Leakage Feedback Gate

A leakage feedback gate holds its state during standby mode by maintaining an active path to one rail contingent on the output. Figure 5 shows the concept at work. When the gate enters sleep, devices M1 and M3 turn off. One of either M2 or M4 also turns off depending on the output of the gate at the time that the sleep signal rises. For example, suppose that out is ’1’ when sleep is asserted. This means that the gates of M2 and M4 are ’0’, so M4 is off and M2 remains on. After the sleep signal turns off devices M1 and M3, the output node connects actively to the VDD rail through M2. The turned-off pair of M3 and M4 disconnect the output node from ground, effectively gating all subthreshold leakage paths with high VT devices. The opposite occurs when out is ’0’. This gate has the interesting property of maintaining its output even when the input node floats. Take the case of the example above. When the gate enters sleep, node in is ’0’. Suppose that in floats to an intermediate value or even to ’1’ once in sleep. The feedback path at the output continues to keep M2 on and M4 off[17].

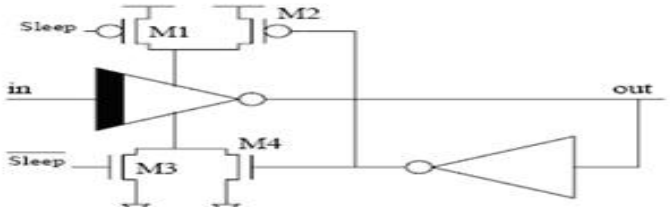

Figure 5 LBFF Technique

d) SOI (Silicon on Insulator)

The elimination of junction capacitance gives SOI improved performance at the same device dimensions and improved subthreshold slopes allows for further device scaling. The floating body of SOI devices is a concern for reliability and circuit simulation [30]. It also causes these devices to have low breakdown voltages which has been a major roadblock to their use in the past, bur as supply voltage continues to scale down this may present less problem.

PROPOSED WORK

The reason to choose this topic is to explore the design methodologies for low power designs and reduce the leakage current which ultimately reduces the power and enhance the performance simultaneously.

In this thesis we are proposing power reduction techniques at circuit level using voltage scaling i.e by optimizing Vdd. At lower Vdd the subthreshold current is increased, to overcome this tox and Capacitance can reduce. We have been implemented a CMOS cell library for digital circuit designs at (0.18 micron and 90 nm) technology using voltage scaling and controlling the subthreshold leakage current without affecting the performance. The techniques are based on the information that, under inversion bias, gate leakage through SiO2 for the PMOS transistors is an order of magnitude lower than for the NMOS [3]. To estimate the power analysis, we are proposing the Conventional CMOS library at 90nm technology. The CONVENTIONAL CMOS CELLS at technologies on 0.35u, 0.25u, 0.18u and 90 nm technologies was designed using Mentor Graphics HEP-2 tool. First we check the performance on each technology & then implemented the Low power CMOS Cell library at 90nm technology using Voltage Scaling and performed Process Corner delay, leakage estimation, load & Temperature analysis to check its performance and then test the logic cells on SCL, STACKING Method, & VTCMOS methods to reduce the subthreshold leakage and optimize the area.

Literature Review

Optimization of power consumption is one of the biggest challenges IC designers face today. Although power optimization has always been critical for battery-operated designs, the continued growth of system performance with each new generation of semiconductor technology, along with the increasing emphasis on "green" and "clean" technical applications, has made power optimization essential even for wall-powered designs.

To understand the facts of power, sources of power, scaling, subthreshold leakage reduction we have selected the following papers for literature review:

1. "Leakage Power Estimation for Deep Submicron Circuits in an ASIC Design Environment", Rahul Kumar,Sasken Communication Technologies Ltd. & C.P. Ravikumar Texas Instruments India Pvt Ltd, HSPICE User's Manual. Vol. II, 1999.

Abstract:-

Rapid progress in the miniaturization of the VLSI technology requires that the supply voltage be scaled down to avoid hot-carrier effects in CMOS logic circuits. The circuit speed gets affected if the ratio of supply voltage VDD to the threshold voltage Vth is less than 5 because the current driving capability of the gates decreases. In order to avoid degradation in speed, the threshold voltage is scaled down. This results in a sharp increase in the standby current. Thus, estimating the dynamic power of CMOS circuits as the only dominant power component is no longer valid. The active power dissipation of the processor core varies significantly depending on the workload, whereas the leakage power dissipation is almost a constant. Since the system remains in the idle state the majority of the time, the contribution of leakage power is far more than that of dynamic power. Chandrakasan et al have made a similar observation after analyzing traces from X-servers [2]; the processor spends more than 95% of its time in standby mode.

Leakage power is thus becoming an important concern for VLSI circuits. Estimation of leakage power is required for gauging and optimizing the total power dissipation of the circuit. What is more, such estimators are most useful in early phases of the design life cycle. This reduces the design cycle time if any optimization at the architectural level is required for leakage power reduction. Most design houses now use an RTL synthesis based flow for designing application-specific integrated circuits. The requirement of such

design houses is a simple estimator which is reasonably accurate and easy to incorporate in the ASIC design flow. This paper proposes such a simple estimator for leakage power.

2. "Low Power Design Techniques for CMOS Circuits & Systems" P.Srinivasulu1, Dr. K.Srinivasa Rao& B. Ananda Babu ,G.I.E.T, MARKAPUR, Prakasam Dist., A.P, INDIA,
Int. J. of Recent Trends in Engineering and Technology, Vol. 4, No. 4, Nov 2010

Abstract:-

Power consumption is a primary concern of designing integrated circuits in deeply scaled CMOS technologies. Present-day technologies possess computing capabilities that make things possible, such as real-time operations. High-speed computation has thus become the expected norm from the average user, instead of being the province of the few with access to a powerful mainframe. Power must be added to the portable unit, even when power is available in non-portable applications, the issue of low-power design is becoming critical. Thus, it is evident that methodologies for the design of high-throughput, low-power digital systems are needed. Techniques for low-power operation are shown in this paper, which use the lowest possible supply voltage coupled with architectural, logic style, circuit, and technology optimizations.

3. **"Analysis of Subthreshold Leakage Reduction in CMOS Digital Circuits" B.S. Deepaksubramanyan and Adrian Nunez EECS Department, Syracuse University, PROCEEDINGS OF THE 13TH NASA VLSI SYMPOSIUM, POST FALLS, IDAHO, USA, JUNE 5-6, 2007.**

Abstract:-

Rapid growth in semiconductor technology has lead to shrinking of feature sizes of transistors using deep submicron (DSM) process. This has allowed for very large circuits with complex functionality to be fabricated on a single chip. As transistor density keeps on increasing so does the power dissipated by the chip. Modern portable battery operated devices such as cellphones, laptops, PDAs are particularly affected by this as high power dissipation reduces battery service life. Thus, power dissipation has now become a vital design metric. Until recently, dynamic or switching power component dominated the total power dissipated by an IC .However, in DSM regime static or leakage power becomes a considerable proportion of the total power dissipation. Leakage power dissipation arises from the leakage currents flowing through the transistor when there are no input transitions and the transistor has reached steady state. The most effective technique for reducing dynamic power dissipation is supply voltage scaling and to maintain performance,

transistor threshold voltage also has to be scaled proportionally. Thus, in the DSM regime due to lower supply voltages, leakage power cannot be neglected. The following are the main sources of leakage currents in DSM circuits : Subthreshold conduction current (ISUB), gate direct tunneling current (IG), gate-induced drain leakage current (IGIDL) and reverse-biased junction leakage current. Amongst all the above listed leakage current components, subthreshold leakage is themost dominant leakage current component. Clearly, the trend follows Moore's law and it is projected that by the year 2020, leakage power is expected to increase 32 times per device .Hence, this necessitates the need for robust techniques to reduce this leakage power dissipation. To this effect, several techniques have been proposed that efficiently minimize leakage power dissipation. This research work analyzes various leakage power reduction techniques applied to current CMOS digital circuits. Of particular focus are static CMOS circuits.

4**." Full-Chip Subthreshold Leakage Power Prediction and Reduction Techniques for Sub-0.18-um CMOS" Siva Narendra, , Vivek De, , Shekhar Borkar, ,Dimitri A. Antoniadis, , and Anantha P. Chandrakasan, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 39, NO. 2, FEBRUARY 2004**

Abstract:-

The driving force for the semiconductor industry growth has been the elegant scaling nature of CMOS technology. In future CMOS technology generations, supply and threshold voltages will have to continually scale to sustain performance increase, control switching power dissipation, and maintain reliability. These continual scaling requirements on supply and threshold voltages pose several technology and circuit design challenges. With threshold voltage scaling, subthreshold leakage power is expected to become a significant portion of the total power in future CMOS systems. Therefore, it becomes crucial to predict and reduce subthreshold leakage power of such systems. In the first part of this paper, we present a subthreshold leakage power prediction model that takes into account within-die threshold voltage variation. Statistical measurements of 32-bit microprocessors in 0.18- m CMOS confirm that the mean error of the model is 4%. In the second part of this paper, we present the use of stacked devices to reduce system subthreshold leakage power without reducing system performance. A model to predict the scaling nature of this stack effect and verification of the model through statistical device measurements in 0.18- m and 0.13- m are presented. Measurements also demonstrate reduction in threshold voltage variation for stacked devices compared to

nonstack devices. Comparison of the stack effect to the use of high threshold voltage or longer channel length devices for subthreshold leakage reduction is also discussed.

5. "**Concurrent Sizing, Vdd and Vth Assignment for Low-Power Design" Ashish Srivastava Dennis Sylvester & David Blaauw, 1530-1591/04 $20.00 (c) 2004 IEEE**

Abstract:-

Using multiple power supplies in a design imposes the topological constraint that gates operating at a lower supply voltage cannot fan-out to gates operating at a higher supply voltage without the use of dedicated level converters. Two approaches that obey this constraint have been proposed in the literature. Early implementations of dual-Vdd designs have showed very promising results with power savings on the order of40-50% . More recently, shows that using a second threshold voltage in conjunction with a second Vdd can be used to maintain the achievable power reduction with scaling process generations. It was also demonstrated that using more than two power supplies or threshold voltages provides minimal reduction as compared to that provided by two Vdd or Vth. This paper is the first to perform simultaneous gate-level sizing, Vdd, and Vth assignment in a dual-Vdd/Vth environment to minimize total power consumption (defined as the sum of static and dynamic power).

6. **"An Implementation of Integral Low Power Techniques for Modern Cell-Based VLSI Designs" A. R. Aswath, M. Puttaraju, and A. B. Kalpana, International Journal of Computer and Electrical Engineering, Vol. 3, No. 3, June 2011.**

Abstract:-

Recent research has proposed several low-power design techniques for VLSI circuitry in nano-scale CMOS era. However, these techniques always involve custom layout design or novel Electronic Design Automation (EDA) flows. In this paper essential low power techniques such as voltage separation, body bias and power switch are implemented in existent place and route (P&R) tools. These techniques enable the possibility to integrated low power techniques into standard Cell-Based physical design flow. The result of these research shows a little overhead in design procedure equally area overhead compare with fully custom design flow. The proposed low power design techniques can be cooperated with modern power management system to enable the power reduction in targeting circuitry with small implementation overheads.

7. "Subthreshold leakage modeling & reduction techniques" James kao, Siva Narendra & Anantha Chanderakasan, 0-7803-7607-2/02/$17.00@2002 IEEE

Abstract:-

As technology scales, subthreshold leakage currents grow exponentially and become an increasingly large component of total power dissipation. CAD tools to help model and manage subthreshold leakage currents will be needed for developing ultra power and high performance

And high power integrated circuits. This paper gives an overview of current research to control leakage currents, with an emphasis on areas where CAD improvements will be needed. The first part of the paper explores techniques to model subthreshold leakage currents at the device, circuit & system levels. Next, circuit techniques such as source biasing, dual Vt portioning, MTCMOS and VTCMOS are described. These techniques reduce leakage currents during standby states and minimize power consumption. In this paper authors are tried to explore ways to reduce total active power by limiting leakage currents and optimally trading off between dynamic and leakage power components.

8. "Leakage current Estimation of CMOS circuits with Stack Effect" , Yong-Jun Xu, Zu Ling You, Xia Wei li, Li xianLi & Xian Long Hong , Journal of Computer Science & Technology, Sept 2005, Volume 19, issue 5.

Abstract:-

Leakage current of CMOS circuits increases dramatically with the technology scaling down and has become a critical issue of high performance system. Subthreshold leakage, Gate leakage and reverse biased band to band tunneling are the important determinants for the leakage current.

In this paper the authors are producing a new model using stacking method and simulate using HSPICE model.

9. **"Power consumption estimation in CMOS VLSI Chips"** Dake Liu & Chrisster Sevensson, IEEE Journal of Solid State Circuits, volume 20, 2004

Abstract:-

Power consumption from logic circuits, interconnects, clock distribution, on chip memories, and off chip driving in CMOS VLSI is estimated. Estimation methods are demonstrated and verified. An estimated tool is created. Power consumption gates, memories and off chip driving are analyzed by examples. In this paper

authors done a comparison between static and dynamic logic and conclude that in dynamic gate array design consumes more power than the cell library design.

10. "Multi-Purpose Technique to Decrease Leakage Power in VLSI Circuits" Gholamreza Karimi, Adel Alimoradi, Canadian Journal on Electrical and Electronics Engineering Vol. 2, No. 3, March 2011

Abstract:-

Motivated by emerging battery-operated application on one hand and shrinking technology of deep submicron (DSM) regime on the other hand, leakage power dissipation is rapidly playing a significant role in the total power dissipation as threshold voltage becomes small. The Low-power design techniques for leakage power minimization are investigated and presented in this paper and then propose a novel method, named ''Multi purpose technique". This method is based on reducing leakage power in activemode with the least delay and the off-state leakage mechanism while saving exact logic state. Library designed using 65nmBSIM4 model of Berkeley Predictive Technology Model (BPTM) has been used to simulate proposed technique compared to investigate techniques.

11. **"Comparison among different CMOS inverter for Low leakage at different Technologies", Vijay Kumar Sharma 1 , Surender Soni, INTERNATIONAL JOURNAL OF APPLIED ENGINEERING RESEARCH, DINDIGUL Volume 1, No 2, 2010**

Abstract:-

In CMOS circuits, the reduction of the threshold voltage due to voltage scaling leads to increase in sub threshold leakage current and hence, static power dissipation. In the nanometer technology regime, power dissipation and Process parameter variations have emerged as major design considerations. These problems continue to grow with leakage power becoming a dominant form of power consumption. On the other hand, variations in the device parameters, both systematic and random, translate into variations in circuit parameters like delay and leakage. Leakage power dissipation is projected to grow exponentially in the next decade according to the International Technology Roadmap for Semiconductors (ITRS). This directly affects portable battery operated devices such as cellular phones and PDAs since they have long idle times. Several techniques used that efficiently minimize this leakage power loss. Stacking is a leakage reduction technique.

12. **“A Novel Leakage Power Reduction Technique for CMOS VLSI Circuits” M. Geetha Priya, K. Baskaran and D. Krishnaveni**

Abstract:-

In recent years, with shrinking of device technologies, leakage power (static power) dissipation has become an inevitable proportion of the total power dissipation in an integrated circuit. The leakage power dissipation is projected to grow exponentially during the next decade according to the International Technology Roadmap for Semiconductors (ITRS). This directly affects portable battery operated devices. In this paper a robust method which is equally effectual for static power control for CMOS VLSI circuits in deep submicron technologies has been proposed. It is also referred to as ‘sleepy pass gate’ uses two complementary sleep transistors connected in parallel forming a pass gate structure. Inour leakage reduction technique, the exact output logic state is preserved in both active and standby mode of operation. Thus, experiments conducted with a range of process technologies on combinational logic gates and MCNC’91 benchmark circuits show that the proposed method gives significant savings in leakage power upto 2 orders of magnitude, with lesser area and delay penalty.

13. **“Design Techniques for Gate-Leakage Reduction in CMOS Circuits” Rafik S. Guindi and Farid N. Najm, 0-7695-1881-8/03 $17.00 Ó 2003 IEEE**

Abstract:-

Oxide tunneling current in MOS transistors is fast becoming a non-negligible component of power consumption as gate oxides get thinner, and could become in the future the dominant leakage mechanism in sub-100nm CMOS circuits. In this paper, we present an analysis of static CMOS circuits from a gate-leakage point of view. We first consider the dependence of the gate current on various conditions for a single transistor, and identify 3 main regions in which a MOS transistor will operate between clock transitions. The amount of gate-current differs by several orders of magnitude from one region to another. Whether a transistor will leak significantly or not is determined by its position in relation to other transistors within a structure. By comparing logically equivalent but structurally different CMOS circuits, we find that the gate current exhibits a ‘structure dependence’. Also, the total gate-leakage in a given structure varies

significantly for different combinations of inputs, from which we derive “state-dependent gate-leakage tables” that can be used to estimate the total amount of gate-current for a large circuit. Finally, we suggest guidelines aimed at reducing the amount of oxide leakage current based on the presented structure and state dependencies.

14. “Circuit-Level Techniques to Control Gate Leakage for sub-100nm CMOS” Fatih Hamzaoglu, Mircea R. Stan, ISLPED ’02, August 12-14, 2002, Monterey, CA, USA.

Abstract:-

Although still negligible for state-of-the-art CMOS, gate leakage will become significant in the future for sub-100nm technologies, due to the scaling of oxide thickness. We propose several circuit techniques to control gate leakage based on the fact that PMOS transistors with SiO2 gate oxide have an order of magnitude smaller gate leakage than NMOS transistors in the same technology. First, we compare n-type domino with p-type domino circuits in terms of performance, leakage and switching power, and explore the different tradeoffs between performance and power. Second, we compare n-type with p-type gating for MTCMOS to control the leakage during sleep. The proposed circuits are simulated for a predictive 70nm CMOS technology with 10Å gate oxide thickness and 1.2V supply voltage.

15. **“A Novel Approach to Reduce the Gate and Sub-threshold Leakage in a Conventional SRAM Bit-Cell Structure at Deep-Sub Micron CMOS Technology” Neeraj Kr. Shukla, R. K. Singh, Manisha Pattanaik, International Journal of Computer Applications (0975 – 8887) Volume 23– No.7, June 2011**

Abstract:-

In the age of scaled silicon technology to improve the functional efficiency of a CMOS design, the device geometry and device parameters are constantly scaled. The major factors of the power consumption due to continuous reduction of the oxide thickness (tOX) is the gate leakage current in both the active and standby mode of the device and other is due to scaled supply voltage, the sub-threshold leakage current. This work proposes a novel approach called as the P3 SRAM Bit -Cell Scheme for the reduction of the active and

standby leakage power through the gate and sub-threshold leakage reduction in the active and standby mode of the memory operation. As the gated transistor is of minimum feature size, so the area penalty is minimum in terms of a large memory and can be compromised. To the best of my knowledge, pMOS Gated-Ground and full-supply voltage body bias for pMOS transistor along with the PP SRAM bit-cell structure is used for the first time in the memory bit -cell design to reduce the power in 45nm CMOS technology at VDD = 0.7V and 0.8V. In comparison with the Conventional and PP SRAM Bit-cells, the active power is achieved for Write Data „0" as 89.21% , 94.38%, and for Write Data „1" as 89.23%, 94.45%, respectively at VDD = 0.7V. When the VDD = 0.8V, the active power is achieved for Write Data „0" as 9.15%, 93.63%, and for Write Data „1" as 91.68%, 93.59%, respectively .

16. **"Statistical Analysis of Subthreshold Leakage Current for VLSI Circuits", Rajeev Rao, Ashish Srivastava& David Blaauw & Dennis Sylvester, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 12, NO. 2, FEBRUARY 2004**

Abstract:-

We develop a method to estimate the variation of leakage current due to both intra-die and inter-die gate length process variability. We derive an analytical expression to estimate the probability density function (PDF) of the leakage current for stacked devices found in CMOS gates. These distributions of individual gate leakage currents are then combined to obtain the mean and variance of the leakage current for an entire circuit. We also present an approach to account for both the inter- and intra-die gate length variations to ensure that the circuit leakage PDF correctly models both types of variation. The proposed methods were implemented and tested on a number of benchmark circuits. Comparison to Monte Carlo simulation validates the accuracy of the proposed method and demonstrates the efficiency of the proposed analysis method. Comparison with traditional deterministic leakage current analysis demonstrates the need for statistical methods for leakage current analysis.

17. "Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicrometer CMOS Circuits" KAUSHIK ROY, SAIBAL MUKHOPADHYAY, HAMID MAHMOODI-MEIMAND, PROCEEDINGS OF THE IEEE, VOL. 91, NO. 2, FEBRUARY 2003

Abstract:-

High leakage current in deep-submicrometer regimes is becoming a significant contributor to power dissipation of CMOS circuits as threshold voltage, channel length, and gate oxide thickness are reduced. Consequently, the identification and modeling of different leakage components is very important for estimation and reduction of leakage power, especially for low-power applications. This paper reviews various transistor intrinsic leakage mechanisms, including weak inversion, drain-induced barrier lowering, gate-induced drain leakage, and gate oxide tunneling. Channel engineering techniques including retrograde well and halo doping are explained as means to manage short-channel effects for continuous scaling of CMOS devices. Finally, the paper explores different circuit techniques to reduce the leakage power consumption

18. "An Analytical Model for Current, Delay, and Power Analysis of Submicron CMOS Logic Circuits" Anas A. Hamoui & Nicholas C. Rumin, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: ANALOG AND DIGITAL SIGNAL PROCESSING, VOL. 47, NO. 10, OCTOBER 2000

Abstract:-

An analytical model for computing the supply current, delay, and power of a submicron CMOS inverter is presented. A modified version of the th power law MOSFET model is proposed and used to relate the terminal voltages to the drain current in submicron transistors. By first computing definable reference points on the output voltage waveform, and then using linear approximations through these points to find the actual points of interest, the desired speed and accuracy of the inverter model are achieved. The most important part of the analysis is a three-step approach for computing the time and output voltage when the short-circuit transistor changes its mode of operation. The time and output voltage when the charging/discharging current reaches its maximum are also calculated and then used to evaluate the propagation delay and characterize the output voltage waveform. The model has been validated for both 0.8 m (5 V) and 0.25 m (2.5 V) CMOS technologies, for a wide range of inverter sizes, input transition times, and capacitive loads. It predicts the

delay, peak supply current, and power dissipation to within a few percent of HSPICE or ELDO simulations based on accurate physically based MOSFET models, while offering about two orders of magnitude gain in CPU time based on a MATLAB implementation.

19. "Design of Low-Power CMOS Cell Structures Using Subthreshold Conduction Region" Vishal Sharma, Sanjay Kumar, International Journal of Scientific & Engineering Research, Volume 2, Issue 2, February-2011 ISSN 2229-5518

Abstract:-

Subthreshold (leakage or cut-off) currents are a necessary evil in traditional VLSI design methodologies. These currents increase exponentially as threshold voltage scales, creating a serious problem for traditional design approaches. This work is based on the exclusive use of subthreshold conduction currents to perform circuit operations, turning this problem into an opportunity. It yields a dramatic improvement in power consumption compared to traditional circuit design approaches. This improvement makes it feasible to design extreme low-power circuits with such an approach. The CMOS digital circuits for this work have been designed using standard TSMC 0.18 *um* Technology.

20. **"Design Technologies for Low Power VLSI", Massoud Pedram Encyclopedia of Computer Science and Technology, 1995**

Abstract:-

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift where power dissipation has become as important a consideration as performance and area. This article reviews various strategies and methodologies for designing low power circuits and systems. It describes the many issues facing designers at architectural, logic, circuit and device levels and presents some of the techniques that have been proposed to overcome these difficulties.

Objective

The objective of this research is to design the Low power CMOS Cell library using power management techniques. The thesis will covers low power design on different design stages at process level and circuit level on the following domains:-

- **Implementation of Conventional CMOS cells on 0.35um, 0.25um & 0.18um technology on HEP2 Mentor Graphics tool.**
- **Comparison of power dissipation in various technology**
- **Implementation of CMOS cells at 90 nm technology.**
- **Simulation results based on power dissipation, temperature, load, timing & process corner analysis using HEP2 Mentor Graphics tool.**
- **Implementation of CMOS cells using Source Coupled logic, Stacking method & VTCMOS technology to optimize the effect of subthreshold leakage on Mentor Graphics tool.**

Work Plan and Methodology

Research work is being carried in the following manner under the supervisor guidance:-

- Review of basics power dissipation basics for Low Power VLSI Design
- Study of Low Power Design Technology
- Study of Various techniques to minimize leakage current at circuit and process level.
- Importance of subthreshold leakage to minimize power consumption and study the various technologies for subthreshold leakage reduction.
- Implementation of various CMOS Cell using transistor sizing, voltage scaling and control leakage using Source Coupled logic , stacking and self bias method at 0.18um and 90 nm technology.
- Simulation and Analysis will perform on spice and mentor graphics tool.
- Future scope of research work.

Conclusion

Scaling down of the CMOS technology feature size and threshold voltage for achieving high performance has resulted in increase of leakage power dissipation. We have presented an efficient methodology for reducing leakage power in VLSI design on proposed CMOS Cells. Throughout logic design, the proposed method could be used to reduce the static power of CMOS circuits. Minimal additional circuitry is used to modify the original logic design to force the combinational logic into a low-leakage state during both active and idle mode of operations.

The thesis starts with detail knowledge of power sources & leakage reduction techniques. It also explains the sub threshold regime operation of MOS and the primary & secondary effects of working in this region. After this in depth description of Voltage Scaling & Source Coupled Logic, the cell library has been proposed and in the end the design & implementation of digital gates using SCL technique has been done. Then simulation results on Conventional CMOS cells using voltage scaling & SCL technique gates is done such as temperature variation, supply variation, load width variation and finally compare with Stacking & VTCMOS method.

CHAPTER ORGANISATION

Abstract

Chapter 1
Introduction
1.1 Historical Perspective
1.2 Motivation
1.3 Objective
1.4 Literature Review
1.5 Conclusion
1.6 References

Chapter 2
Low Power CMOS VLSI Design
2.1 Power Sources in VLSI circuit
2.2Power Reduction techniques of CMOS
2.4 Subthreshold Leakage reduction techniques
2.5Conclusion

Chapter 3
Sub threshold MOS for Low Power
3.1 MOS Technology
3.2Device Modeling
3.3 Design Consideration in Subthreshold
3.4 Low Power design using Subthreshold MOS
3.5 Conclusion

Chapter 4

Implementation, Analysis & Simulation of the Proposed Low Power CMOS Cells
4.1 Review of Leakage reduction technique
4.2 Proposed CMOS Cell Library with simulation results at 90nm technology

- NOT Gate
- NOR Gate
- NAND Gate
- XOR Gate
- XNOR Gate
- Half Adder
- Full Adder
- Half Subtractor
- Full Subtractor
- MUX
- Decoder
- Flip Counters
- Flop

4.3 Performance & Comparative Evaluation of logic gates of 0.35 to 90 nm technology through various analyses

- Load Analysis

- Power Dissipation
- Temperature Analysis
- Process Corner Analysis
- Delay Analysis
- Area Estimation of the Cells

Chapter 5

Proposed subthreshold leakage reduction technique for CMOS Cells

5.1 Source Coupled Logic
5.2 Various logic gates designing using SCL
5.3 Various analyses on SCL Inverter
5.4 Simulation Results of SCL
5.5 Leakage power for different SCL gates
5.6 Stacking Method
5.7 VTCMOS Method
5.8 Summary

Chapter 6

Conclusion

6.1 Thesis Contribution
6.2 Future Scope
6.3References & Bibliography
6.4 Publications

Paper Published in National & International Journal

S.No.	Title of the Paper	Journal /Conference	Author/s	Year	Vol./Issue	ISSN No.	Impact Factor
1.	CMOS Low power cell library for digital design	VLSICS, Springer	Kanika Kaur, Arti Noor	June 2013	**Volume 4. Issue 3**	0976-1357(O) 0976-1527(P)	1.0
2.	Performance of Low Power SRAM Cells on SNM and Power Dissipation	International Journal of Emerging Trends & Technology in Computer Science (IJETTCS)	Kanika Kaur, Anurag Arora	April 2013	Volume 2, Issue 2, March – *April* 2013 pp.15-19	ISSN 2278-6856	2.524
3.	Corner & Delay Analysis of Low Power CMOS Cells	International Journal of Electrical & Electronics Engineering @TJPRC	Kanika Kaur, Arti Noor	Jan-Mar 2013	Vol. 3, Issue 1, pp. 161-168	ISSN: 2278-943x	5.7567
4.	32bit ALU design using FPGA	International Conference in Electrical and Electronics Engineering , at JNU Campus ,Delhi and & published in International Journal of Electrical and Electronics Engineering	Kanika Kaur, Shikha Khurana	Sept.2012	Volume 5, Number 8,		1.0
5.	WIRELESS WATER LEVEL INDICATOR WITH POWER SAVER	International Conference in Electrical and Electronics Engineering , at JNU Campus ,Delhi and & published in International Journal of Electrical and Electronics Engineering	Kanika Kaur, Pulkit Verma, Moumita	Sept.2012	Volume 5, Number 8,		1.0
6.	ALU Implementation using FPGA	International Journal of Emerging Trends & Technology in Computer Science (IJETTCS)	Kanika Kaur, Shikha Khurana	August 2012	Volume 3, Issue 2,pp 146-149	ISSN 2278-6856	2.56
7.	Comparative analysis Power Estimation for CMOS Cell	International Journal of Contemporary Research in Engg. and Tech(IJCRET) , special issue of VLSI	Kanika Kaur	July2012	Volume2, Issue1,pp26-33	ISSN: 2250-0510	1.3
8.	Power Estimation Analysis for CMOS Cell Structures	International Journal of Advances in Engineering & Technology (IJAET)	Kanika Kaur, Arti Noor	May, 2012	Vol. 3, Issue 2, pp. 293-301	ISSN: 2231-1963	2.5
9.	Minimization of Leakage Current in VLSI design	International Journal of Scientific and Engineering Research(IJSER)	Kanika Kaur, Arti Noor	April-2012	Volume 3, Issue 4,pp. 201-205	ISSN 2229-5518	1.4

10	Function Generator Designing using Second Generation Current Conveyor	International Journal of Applied Engineering Research (IJAER)	Kanika Kaur, Arti Noor	Nov.2011	Volume 6, Number 18 (2011) pp. 2145-2157	ISSN 0973-4562	1.7
11	STRATEGIES & METHODOLOGIES FOR LOWPOWER VLSI DESIGNS: A REVIEW	International Journal of Advances in Engineering & Technology (IJAET	Kanika Kaur, Arti Noor	May 2011	Vol. 1,Issue 2,pp.159-165	ISSN: 2231-1963	2.5

Research Papers Published / Presented in National & International Conferences

1) Presented a paper titled **"Carrier Prospectus in VLSI Design"** at Northern India Engineering College, Delhi in the National Seminar on **"Recent Development in VLSI Design"** on 25th January 2007.

2) Presented a research paper titled **"RTL Power Reduction Techniques"** in the National Conference on **"Technology for Rural India- Challenges and Perspective"** on ISTE Day-2008 at NSIT Campus, New Delhi on 31st May & 1st June 2008.

3) Published a research paper titled **"Bluetooth Scatter net Technology" , Kanika Kaur, Vishamhar Nath ,S.C.Gupta** in the National Conference on **"Emerging trends in Embedded Technology (ETET-2009)"** at SGIT Campus, Gzb on 14th February 2009.

4) Published a research paper titled **"FPGA synthesis process for Embedded Technology",**Kanika Kaur, Mukul Chauhan, Navneet Kumar in the National Conference on **"Emerging trends in Embedded Technology (ETET-2009)"** at SGIT Campus, Gzb on 14th February 2009.

5) Published a research paper titled **"**Image Decomposition, **Reconstruction and Denoising using wavelet transform and matlab",** Kanika Kaur, Mukul Chauhan, Navneet Kumar in the National Conference on **"Emerging trends in Embedded Technology (ETET-2009)"** at SGIT Campus, Gzb on 14th February 2009.

6) Presented a research paper titled **"FPGA Reconfigurable Technique for Embedded system",** Kanika Kaur in the National Conference on **"Future Trends in Application of Computers in Science & Technology (ACST-2009)"** at IMs College of Engineering, Gzb during Feb 7-8, 2009.

7) Presented a research paper titled **"PLDs Reconfigurable Technique for Embedded system",**Kanika Kaur in the National Conference on **"Emerging Trends in Electronics & Computers Engineering"** at Lingya's Institute of technology, 21st – 23rd march 2009.

8) Presented a research paper titled **"Synthesis Method for Field Programming Gate Arrays",**Kanika Kaur, Jasbeer Kaur in the National seminar on **"Advancements in VLSI Technology(VLSITEK-2010) ,** at MAIT College of Engineering, Gzb, , 25th march 2010.

9) Published a research paper titled **"INTEGRATED CIRCUIT LOGARITHMIC DIGITAL QUANTIZERS WITH APPLICATIONS TO LOW-POWER DATA INTERFACES FOR SPEECH PROCESSING"** Kanika Kaur, M.P.Tripathi in the National seminar on **"Advancemen in VLSI Technology (VLSITEK-2010) ,** at MAIT College of Engineering, Gzb, , 25th march 2010.

10) Published a research paper titled **"Quality of EDA CAD Tools: Definitions, Metrics and Direction"** Kanika Kaur, S.C.Gupta in the National seminar on **"Advancements in VLSI Technology (VLSITEK-2010) ,** at MAIT College of Engineering, Gzb, , 25th march 2010.

11) Presented a research paper titled **"LOGARITHMIC DIGITAL QUANTIZERS FOR SPEECH PROCESSING"** Kanika Kaur, in the National Conference on **"Electronics Communication and Instrumentation- EMANTHAN-2010" at College of Sciences and Engineering, Jhansi** during 1st and 2nd April 2010.

12) Presented and published research paper titled **"FPGA Based Low Power System DesignTechniques" technically supported by IEEE, IETE& CSI.** in the national conference **"NCET-2010 "** dated 22nd -23rd Nov 201o at Arya College of Engineering and technology, Jaipur, Rajasthan.

13. Presented and published research paper titled **"Current Minimization Technique for CMOS Circuits"** in the **conference** "**ICACTEA-2011" technically supported by IEEE,IETE & ISTE** dated 24th -26th Feb 2011 at Poornima College of Engineering, Jaipur, Rajasthan.

14. Published research paper titled **"Carbon Nano Tubes Sensors Networks: a review"** Preeti, Deepak Tiwari & Kanika Kaur in the National Seminar **on "Applications of Nanotechnology for Environment and Technical Development - ANETD -2011"** at KIIT College of Engineering, Gurgaon on 11th Feb 2011.

15. Research Paper titled **"32bit ALU design using FPGA"** presented in International **Conference "Emerging trends in Electrical and Electronics and Communication Engineering, held at JNU, New Delhi on 29-30 September 2012.**

16. Research Paper titled **"WIRELESS WATER LEVEL INDICATOR WITH POWER SAVER"** presented in International **Conference "Emerging trends in Electrical and Electronics and Communication Engineering, held at JNU, New Delhi on 29-30 September 2012 .**

17**.** Research Paper titled **"FPGA Implementation of low power Cell library for digital design"** presented in National **Conference "**"INDIACOM-2013 At BVICAM, New Delhi Technical Sponsored by IEEE, Delhi ,IETE, IE Delhi Centre, ISTE & CSI Region1 on from 7-8 march 2013

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